(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 862 219 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
02.09.1998 Bulletin 1998/36

(51) Int. Cl.[6]: **H01L 27/146**, H04N 3/15

(21) Application number: **98200441.8**

(22) Date of filing: **12.02.1998**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **28.02.1997 US 808444**

(71) Applicant: **EASTMAN KODAK COMPANY**
Rochester, New York 14650 (US)

(72) Inventor:
Guidash, Robert Michael,
c/o Eastman Kodak Company
Rochester, New York 14650-2201 (US)

(74) Representative:
Parent, Yves et al
KODAK INDUSTRIE,
Département Brevets,
CRT - Zone Industrielle
71102 Chalon-sur-Saône Cedex (FR)

(54) Active pixel sensor in which adjacent pixels share an integrated electrical element

(57) An image sensor having a plurality of pixels comprising a semiconductor material of a first conductivity type with at least two adjacent pixels, each of the pixels has a photodetector formed within the substrate and an electrical function that is shared between the adjacent pixels integrated within the adjacent pixels. The electrical function can be: a transfer gate, a reset gate, a row select gate, an amplifier drain, an output node, a floating diffusion, a reset drain, a lateral overflow gate, an overflow drain or an amplifier, that is shared between multiple pixels resulting in a saving of space.

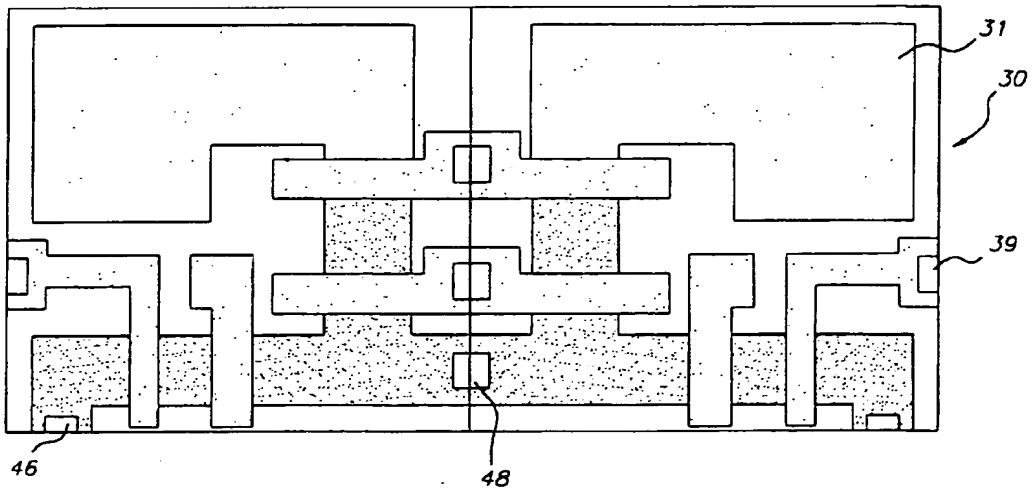

FIG. 4A

EP 0 862 219 A2

Description

FIELD OF THE INVENTION

The invention relates generally to the field of solid state image sensors, specifically imagers referred to as Active Pixel Sensors, (APS), and to providing greater fill factors within APS sensors.

BACKGROUND OF THE INVENTION

Description of the Prior Art

APS are solid state imagers wherein each pixel typically contains a photo-sensing means, reset means, a charge transfer means, a charge to voltage conversion means, and all of part of an amplifier. Prior art APS devices have been operated in a manner where each line, or row, of the imager is selected and then read out using a column select signal (analogous to the selection and reading of a memory device). In prior art devices the connection, or contact, to the various nodes within the pixels of a given row is accomplished on a per pixel basis. This is true even though the pixels exist on the same electrical node within a row (see Fig. 1). Since these contact regions are placed in each pixel, and contact regions typically consume a large amount of pixel area due to the overlap of metal layers required, inclusion of these contact regions in each pixel reduces the fill factor for the pixel because it yes up area that could otherwise be used for the photodetector. This reduces the sensitivity and saturation signal of the sensor. This adversely affects the photographic speed and dynamic range of the sensor, performance measures that are critical to obtaining good image quality. In addition prior art APS pixels have included the entire amplifier, address and reset transistors within a single pixel, and have made operative interconnection of these components and the photodetector entirely within a single pixel boundary. This leads to inefficiencies of layout and produces pixels with small fill factors.

In order to build high resolution, small pixel APS devices, it is necessary to use sub-mm CMOS processes in order to minimize the area of the pixel allocated to the row select transistor and other parts of the amplifier in the pixel. In essence, it takes a more technologically advanced and more costly process to realize the same resolution and sensitivity in an APS device as compared to a standard charge coupled device (CCD) sensor. However, APS devices have the advantages of single 5V supply operation, lower power consumption, x-y addressability, image windowing, and the ability to effectively integrate signal processing electronics on-chip, when compared to CCD sensors.

A typical prior art APS pixel 10 is shown in Fig. 1. The pixel comprises a photodetector (PDET) 11, that can be either a photodiode or photogate, a transfer gate (TG) 12, floating diffusion (FD) 14, reset transistor with a reset gate (RG) 16, row select transistor with a row select gate (RSG) 4, and signal transistor (SIG) 5. Note that all of the electrical components required to readout and address the pixel are contained entirely within a single pixel boundary, and are operatively connected entirely within a single pixel boundary. Regions to provide contact to each of the various electrical nodes within the pixel that are common to a row are designated in Fig. 1 and shown schematically in Fig. 2. These are Transfer Gate Contact (TGC) 13, Reset Gate Contact (RGC) 17, and Row Select Gate Contact (RSGC) 3. Additionally there are contact regions that are common to a column. These are also shown in Figs. 1 and 2. These are power supply contacts (VDDC) 9 and the pixel output node contact (OUTC) 8. Note that there are separate and individual contact regions in each pixel even though some are common to a row or column. It is evident that the area consumed by these contact regions is a significant portion of the pixel area, thus limiting the area available for the photodetector, which reduces the fill factor and sensitivity of the pixel.

It should be apparent, from the foregoing discussion, that there remains a need in the art for APS sensors that have increased fill factors. This and other problems are addressed by the present invention.

SUMMARY OF THE INVENTION

The present invention addresses the foregoing problems. Briefly summarized, according to one aspect of the present invention the an image sensor having a plurality of pixels comprising: a semiconductor material of a first conductivity type; and at least two adjacent pixel having photodetectors formed within the substrate such that each pixel has at least one electrical function that is shared by the adjacent pixels.

The pixel layout innovation provided by the present invention yields a higher fill factor for the pixel. One approach to providing an image sensor with the sensitivity of a CCD and the advantages of an APS device is to improve the fill factor, thereby, increasing the corresponding sensitivity of the APS device. This is accomplished by the present invention in several ways: first by eliminating the need for a separate signal line contact areas in each pixel. Secondly, by sharing electrical components between pixels. Finally, fill factor can be increased by operatively interconnecting the electrical components by traversing pixel boundaries and using the array to complete the routing. These are all accomplished while maintaining the ability to selectively address specific pixels of the APS device.

The invention provides a means for reducing the area per pixel required for these contact regions. Conceptually, it can be described in the following manner. The design of each pixel is done to place the contact regions of the row related nodes along or near the left and right edges of the pixel, and the column related contact regions along or near the top or bottom edge of the

pixel, (see Fig. 3), allowing neighboring pixels to share these contact regions and alleviating the requirement of having separate contact regions in each pixel. In the case of the preferred embodiment of the present invention, contact regions are required for every 2 pixels as compared to each pixel as required by prior art devices. Hence, the area required per pixel by the present invention is reduced, resulting in an increase in fill factor for the pixel.

Additionally, one can use the VDD drain region of an adjacent pixel as a lateral overflow drain. This is a similar "pixel sharing" concept where the VDD drain region serves as the drain of the signal transistor for one pixel and the lateral overflow drain for the adjacent pixel or pixels. Since a separate lateral overflow drain region is not needed for each pixel, more area can be allocated to the photodetector, providing increased fill factor.

Another means to realize fill factor improvement is to utilize the row at a time read out operation, and provide a floating diffusion and amplifier for every two pixels instead of for each pixel. Since only one row is read out at a given time, a single floating diffusion and amplifier can be used for 2 adjacent pixels that are in separate rows. Once again the photodetector area per pixel can be increased, or the fill factor can be maintained to produce a smaller pixel.

Finally, by operatively interconnecting the pixel components such that the components orientation traverse pixel boundaries (rather than providing a schematically complete layout within a single pixel boundary) layout efficiencies can be utilized to improve the fill factor of the pixel.

These and other aspects, objects, features, and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

Advantageous Effect Of The Invention

The present invention has the following advantages. All of the features and advantages of prior art APS devices are maintained while requiring less pixel area for contact regions. This provides the following advantages:

higher fill factor, sensitivity and saturation signal for the same pixel size;
smaller pixel and device size for the same fill factor.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top view of prior art APS pixel;

Fig. 2 is a schematic of an array of four prior art pixels as shown in FIG. 1;

Fig. 3 is a top view of a pixel as envisioned by the present invention; having reduced contact area;

FIG. 4A is a top view of two pixels of the present invention that illustrates the sharing of contact regions;

FIG. 4B is a top view of the present invention as shown if FIG. 4a with reduced VDD contact region;

FIG. 5A is a top view of 4 pixels of the present invention that are a mirror duplication of the two pixels in FIG. 4A that illustrates the sharing of contact regions that are common to a column;

FIG. 5B is a top view of 4 pixels of the present invention that are a mirror duplication of the two pixels in FIG. 4B that illustrates the sharing of contact regions that are common to a column;

FIG. 6 is the pixel of FIG. 4A that includes a lateral overflow gate and drain;

FIG. 7 is a diagram of 2 of the pixels as shown in FIG. 4A with a lateral overflow gate for each pixel and VDD of the adjacent pixel used as a lateral overflow drain;

FIG. 8 is an illustration of 2 pixels sharing floating diffusion, reset gate, reset drain VDD, amplifier, row select gate, and output contact region.

FIG. 9 is a top view of 4 pixels illustrating operative interconnection of electrical components across pixel boundaries.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION OF THE INVENTION

One physical embodiment of the new pixel architecture is shown in Fig. 3. Other specific physical embodiments are realizable. This one is chosen for illustration. The pixel 30 has a photodetecting area 31 that accumulates charge from incident light and transfers the stored charge under control of the transfer gate 32 to a floating diffusion 34.

There are various contact regions that are associated with the circuit elements recited within the above description. The transfer gate 32 has a transfer gate contact 33, the reset gate 36 has a reset gate contact 37 and the row select gate 38 has a row select gate contact (RSGC) 39. These contact regions are row common contact regions, and are placed appropriately along the left and right side of pixel 30 boundaries. In the preferred embodiment as shown if FIG. 3, half of the con-

tact region for reset gate contact 37 and transfer gate contact 33 are placed on the left edge of the pixel. Half of a contact region for the row select gate contact 39 is placed along the right edge of the pixel. Next the column common contact regions VDDC 40 and OUTC 41 are placed appropriately along the bottom edge of the pixel. This architecture allows these various elements to be shared between pixels, in terms of function and also in terms of pixel area used to construct these elements.

An array of pixels is then constructed in the following manner. First, a new pixel is created by mirroring the original pixel in the x-dimension. The new pixel is then butted with the original pixel by placing the half contact regions adjacent to each other. This is shown in Figs. 4A and 4B. In Fig. 4A, VDDC 48 is shared by 2 pixels. OUTC 46 is placed along a pixel border so that it may be shared with another pixel. In Fig. 4B, VDDC 49 is placed along the bottom edge of the pixel so that it can be shared by 4 pixels. This can be done since the VDDC 49 node is common to all pixels, rows and columns. OUTC 47 is placed along a pixel border so that it may be shared by another pixel. Next this group 2 pixels mirrored in the y-dimension then created another set of 2 pixels. These sets of 2 pixels are then butted so that the half contact regions for VDDC and OUTC are adjacent to each other. This is shown in Figs. 5A and 5B, corresponding to Figs. 4A and 4B, respectively. This set of 4 pixels is then arrayed to produce the desired number of pixels in the image sensor.

In order to provide antiblooming control during readout of the sensor, it is necessary to provide an overflow drain for the photodetector. The simplest approach in a CMOS process is to provide a lateral overflow drain that is separated from the photodetector 31 by a gate 65. If one were to include a lateral overflow drain 66 in each pixel, this would further reduce the fill factor of the pixel, and adversely affect the sensitivity of the pixel. This is shown in Fig. 6. However, by placing the VDD region appropriately within the pixel, this can be used as the lateral overflow drain for the adjacent pixel or pixels. One example of this is shown in Fig. 7. Since the lateral overflow drain 66 is now in another pixel, the pixel fill factor is not affected. By using this approach, antiblooming control during readout is achieved without impacting pixel fill factor.

Finally, Fig. 8 illustrates a new design of a pixel 80 that shares the floating diffusion 84, amplifier 85, row select transistor 86, and reset gate 87 with an adjacent pixel that is in a separate row. In this case the row select signal for 2 consecutive rows is actually the same. Image signal separation is achieved by having separate Transfer Gates 81, 82 in each pixel. The operation occurs in the following manner. Row A is integrated, and the gate of the row select transistor 85 is turned on. The floating diffusion 82 is then reset by pulsing the reset gate 87. This reset signal is then read out for row A. Transfer Gate 81 is then pulsed on and the signal charge from photodetector A is transferred onto the floating diffusion 84. The signal level is the read out for row A. Next the floating diffusion 84 is reset by pulsing on reset gate 87 again. The reset level for row B is then read out. TGB is then pulsed on to transfer the signal charge from photodetector B onto the floating diffusion. The signal level is then read out for row B. This procedure is then repeated for the remaining pairs of rows on the device.

Fig. 9 is a top view of 4 pixels of the present invention illustrating the concept of routing or interconnecting across pixel boundaries. A contact region for the signal transistor is placed to the right side of the floating diffusion and ends at the right side of the pixel boundary 90. When another pixel is butted to the right side, this completes the connection of the floating diffusion to the signal transistor. This is done similarly with the reset gate using the top and bottom boundaries of the pixel. This concept provides the ability to have minimum routing and interconnect area.

Although not shown in these examples, it is desirable to design the pixel so the photodetector occupies the same site within the pixel even when the pixel is mirrored so the modulation transfer function of the imager is constant throughout the device.

It should be noted that although not shown in the drawings, each of the features detailed in this invention can be used in conjunction with each other to produce other physical layouts and embodiments that provide the advantages discussed.

The invention has been described with reference to a preferred embodiment, however, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention.

PARTS LIST:

3	row select gate contact 3
4	row select transistor
5	signal transistor
8	output node contact
9	power supply contact (VDDC)
10	prior art pixel
11	photodetector
12	transfer gate
13	transfer gate contact
14	floating diffusion
16	reset gate
17	reset gate contact
30	pixel
31	photodetector
32	transfer gate
33	transfer gate contact
34	floating diffusion
36	reset gate
37	reset gate contact
38	row select gate
39	row select gate contact

40 VDDC
41 OUTC
45 OUTC
46 OUTC
47 OUTC
48 VDDC
49 VDDC
65 lateral overflow gate
66 lateral overflow drain
80 pixel
81 transfer gate contact
82 transfer gate
84 floating diffusion
85 amplifier
86 row select transistor
87 reset gate
90 pixel boundary

Claims

1. An image sensor having a plurality of pixels comprising:

   a semiconductor material of a first conductivity type;

   at least two adjacent pixels each of the pixels having photodetectors formed within the substrate; and

   at least one electrical function integrated within the adjacent pixels that is shared between the adjacent pixels.

2. The image sensor of claim 1 wherein the shared electrical function further comprises a shared contact region.

3. The image sensor of claim 1 wherein the shared function further comprises a shared electrical component.

4. The image sensor of claim 1 wherein the shared function further comprises a shared contact region but not a shared electrical component between the adjacent pixels.

5. The image sensor of claim 1 wherein the shared function further comprises both a shared contact region and a shared electrical component.

6. The image sensor of claim 1 further comprising a voltage supply of one pixel that is also used as an overflow drain for the adjacent pixel.

7. An image sensor having a plurality of pixels comprising:

   a semiconductor material of a first conductivity type; and

   at least two adjacent pixels having photodetectors formed within the substrate such that each pixel has at least one electrical component integrated within the pixels that is shared by the adjacent pixels.

8. An image sensor having a plurality of pixels comprising:

   a semiconductor material of a first conductivity type; and

   at least two adjacent pixels each having photodetectors formed within the substrate such that each pixel has at least one electrical component that is functionally associated with one of the adjacent pixels and at least a portion of the electrical component is structurally located within the pixel boundary of the other adjacent pixel.

9. An image sensor having a plurality of pixels comprising:

   a semiconductor material of a first conductivity type;

   at least two adjacent pixels having photodetectors formed within the substrate such that each pixel has at least one electrical component integrated within the pixel; and

   a contact region that is shared by the electrical components of the adjacent pixels.

10. A method of making solid state image sensing devices comprising the steps of:

    providing a substrate made from a semiconductor material of a first conductivity type having a plurality of pixels formed on a major surface of the substrate such that there are at least two adjacent pixels each having photodetectors formed within the substrate; and

    further providing at least one electrical function integrated within the adjacent pixels that is shared between the adjacent pixels.

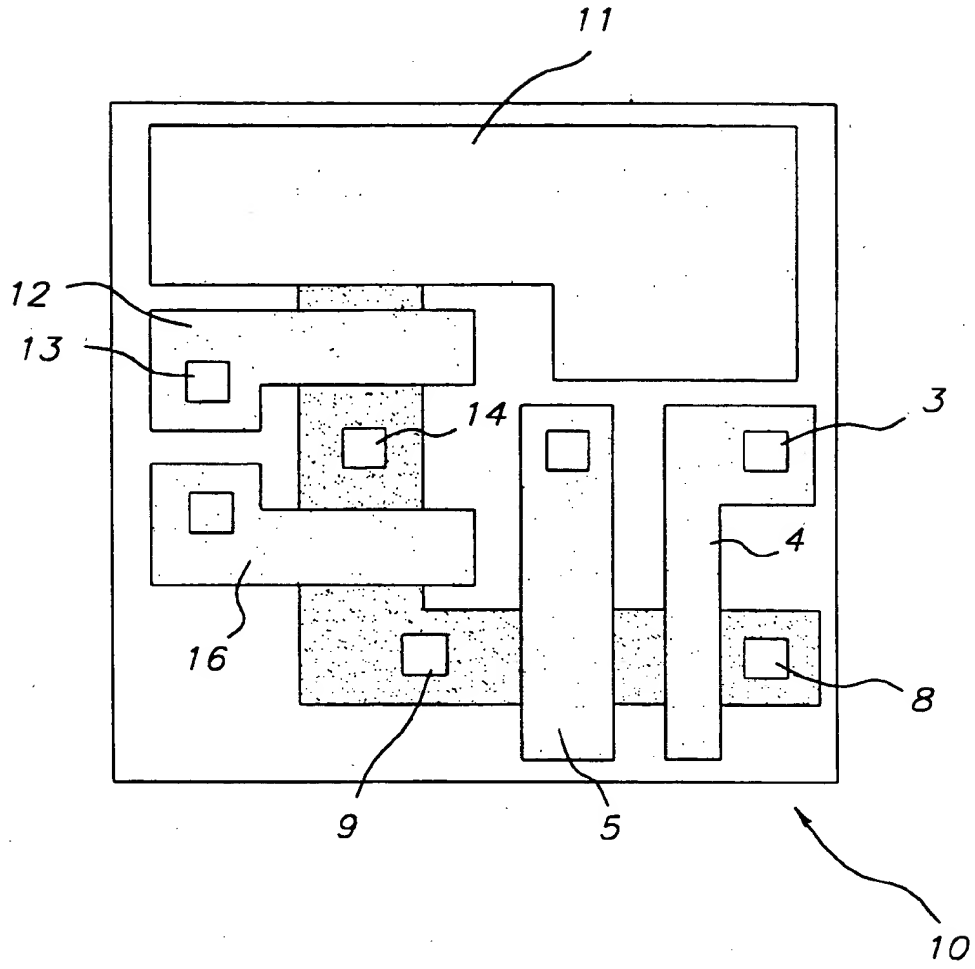

FIG. 1
(PRIOR ART)

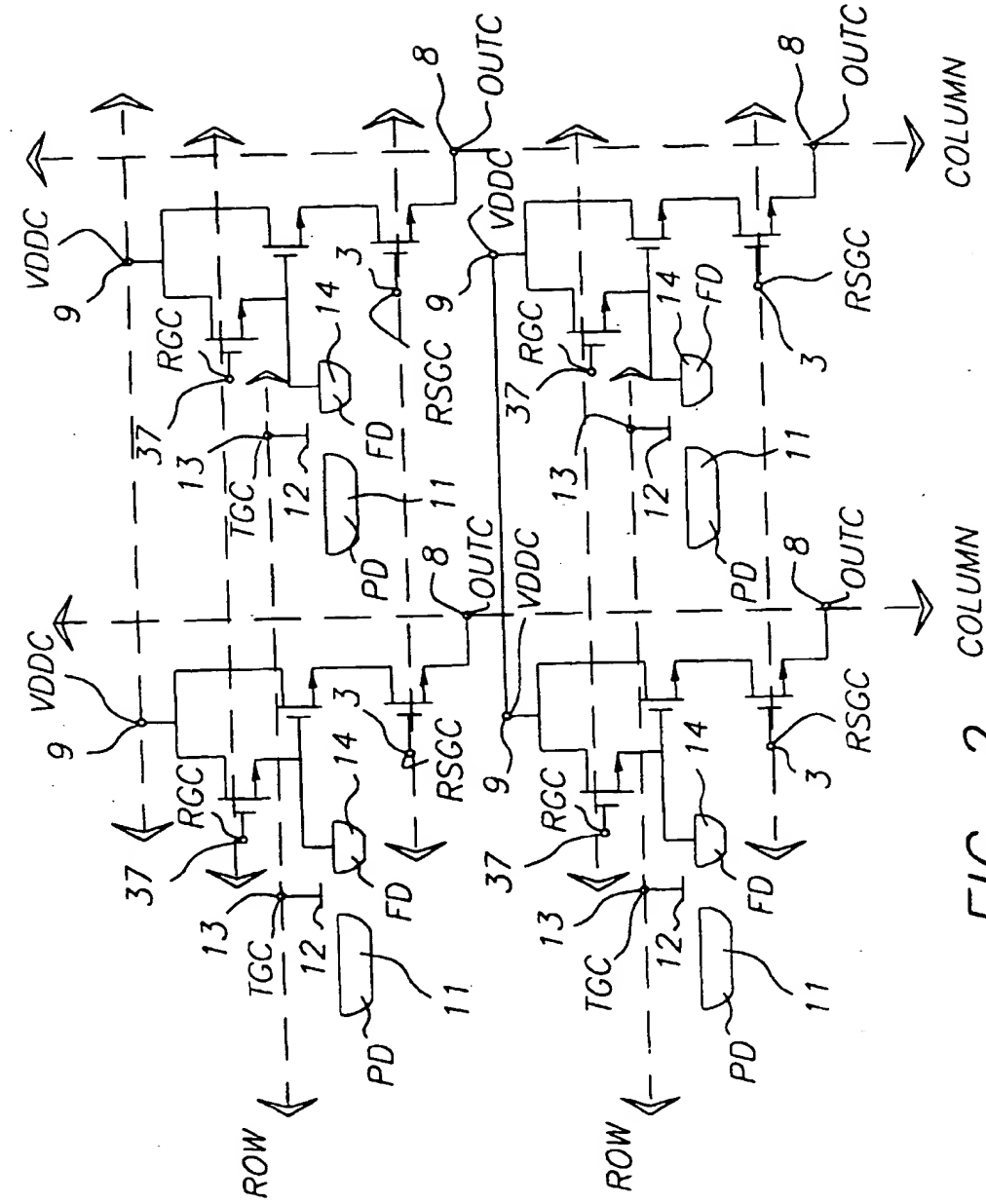

FIG. 2
(PRIOR ART)

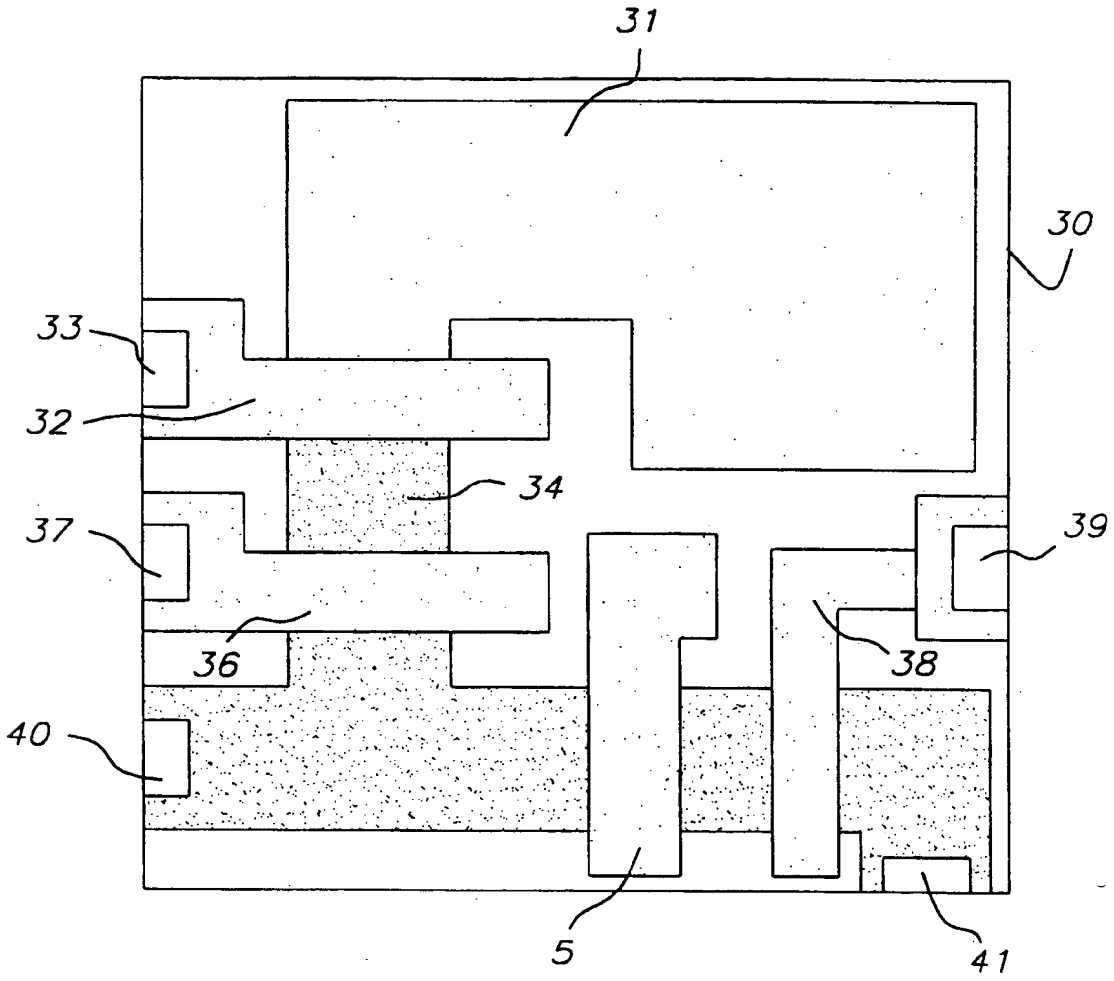

FIG. 3

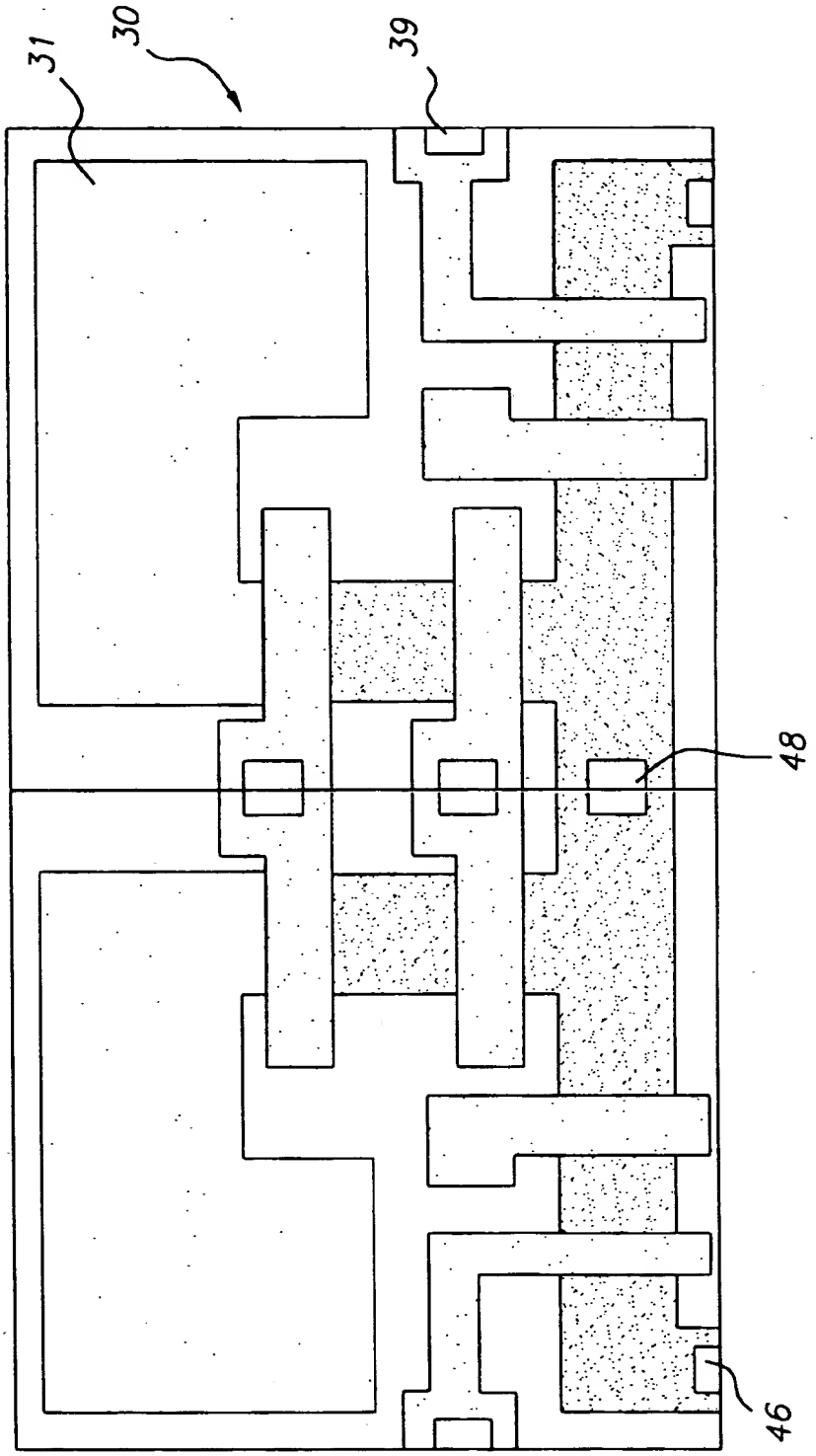

FIG. 4A

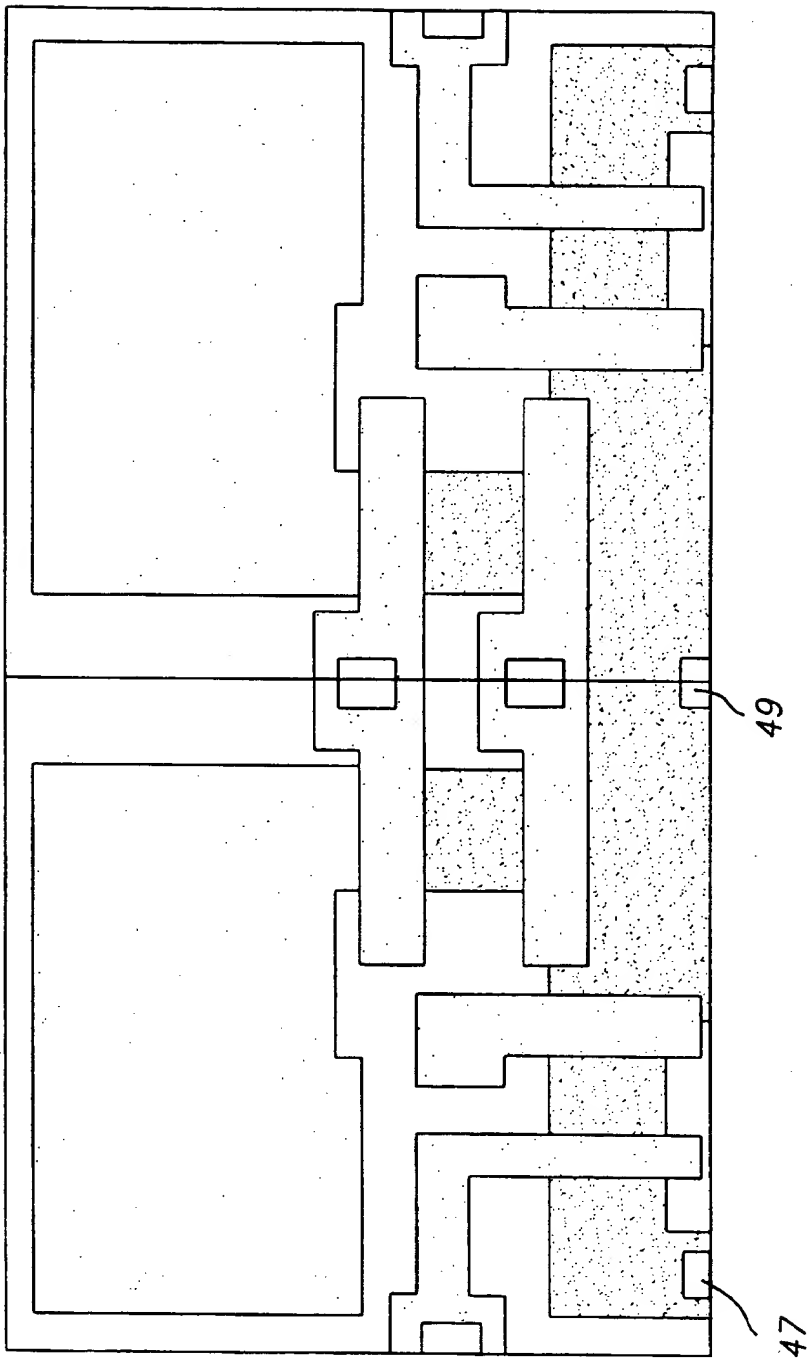

FIG. 4B

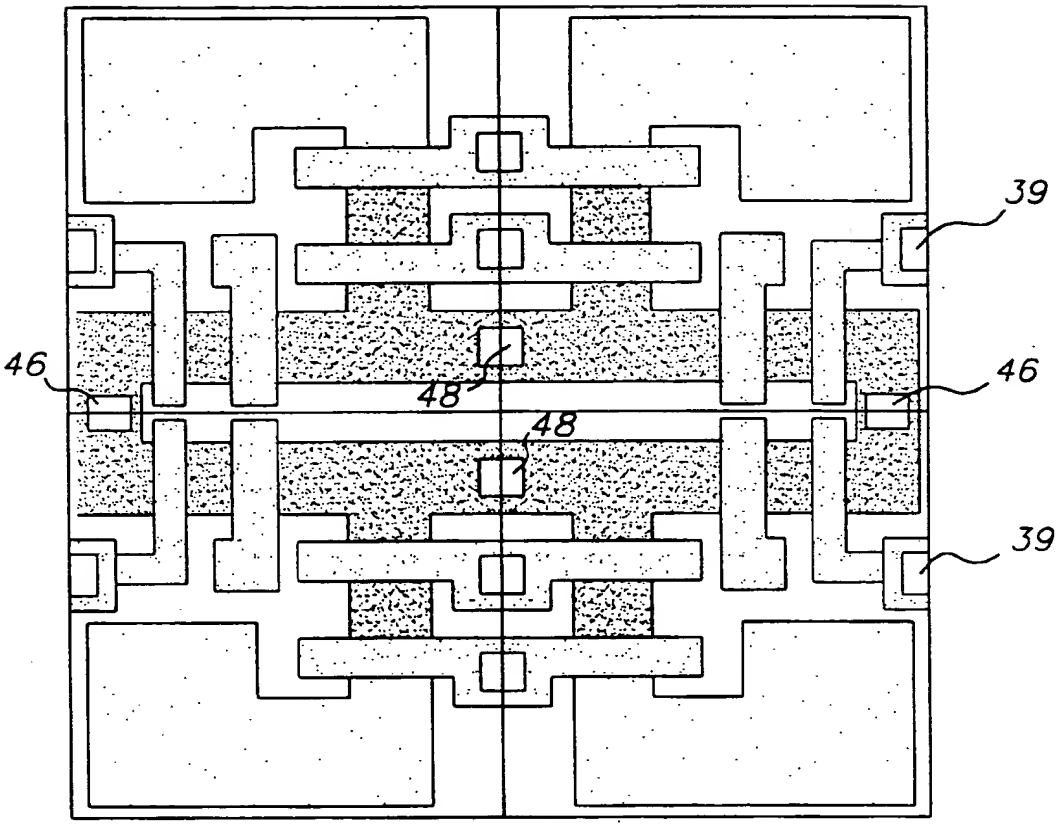

FIG. 5A

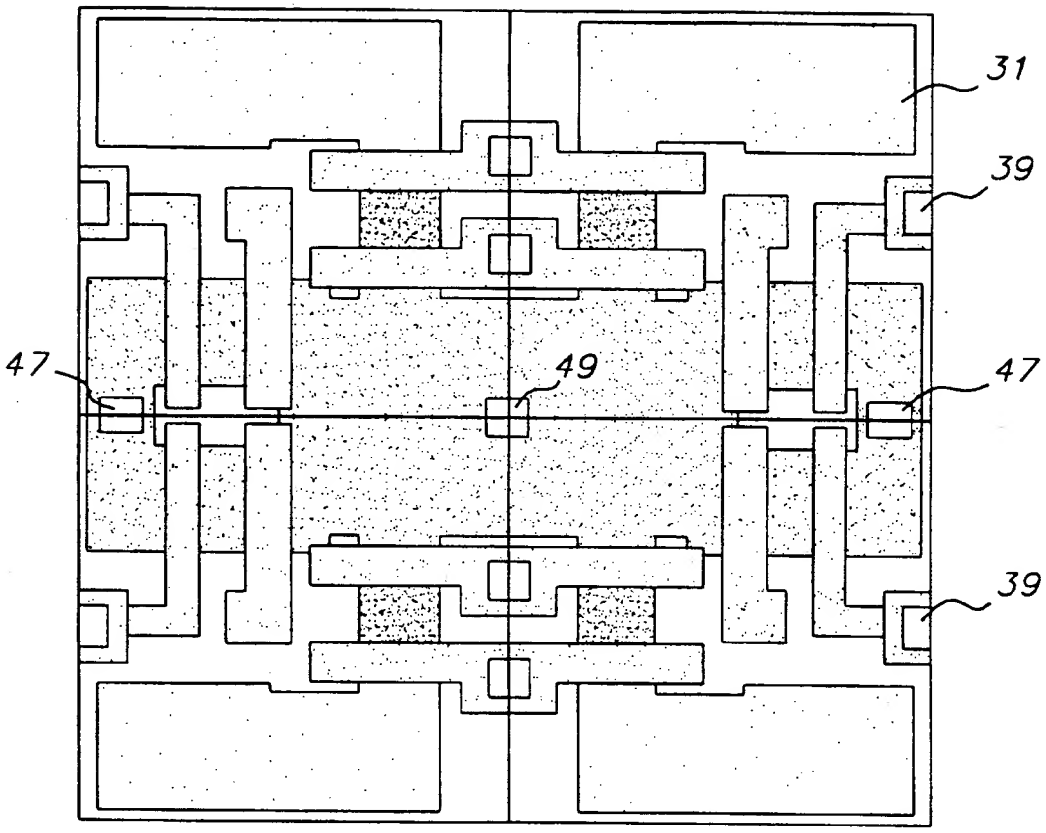

FIG. 5B

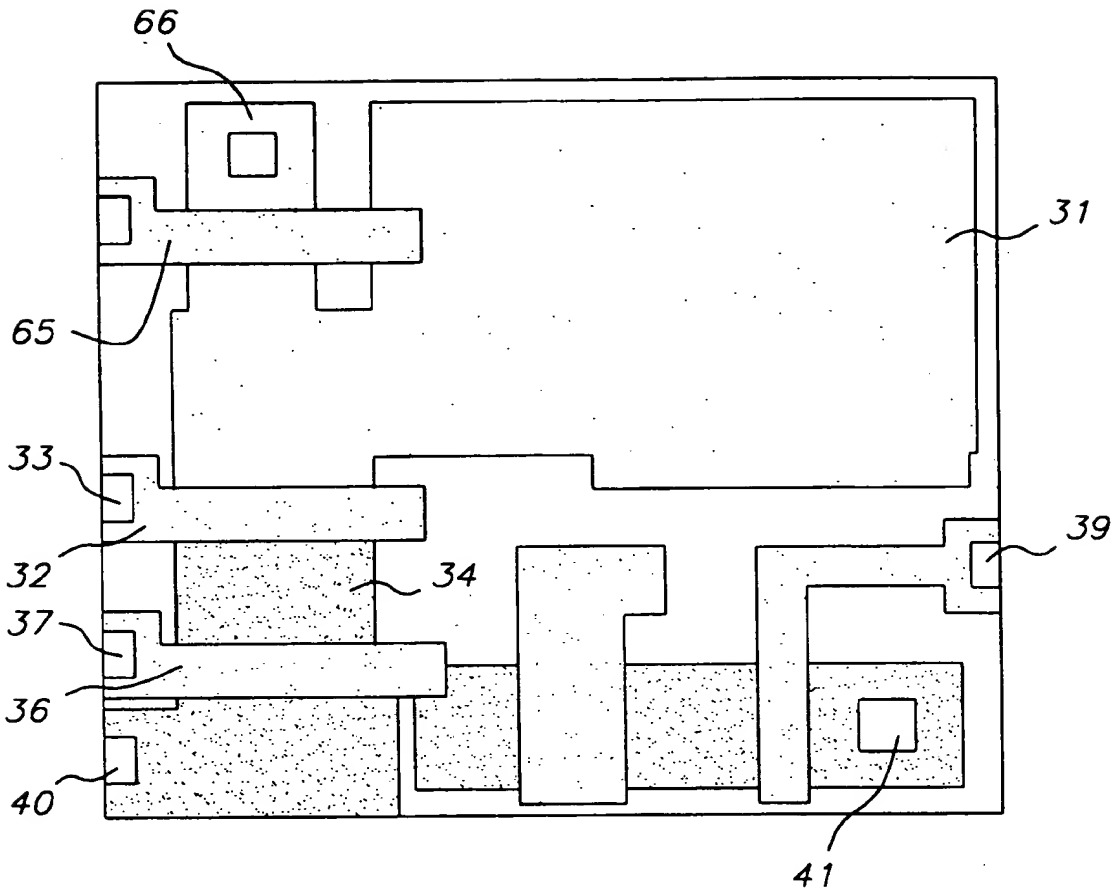

FIG. 6

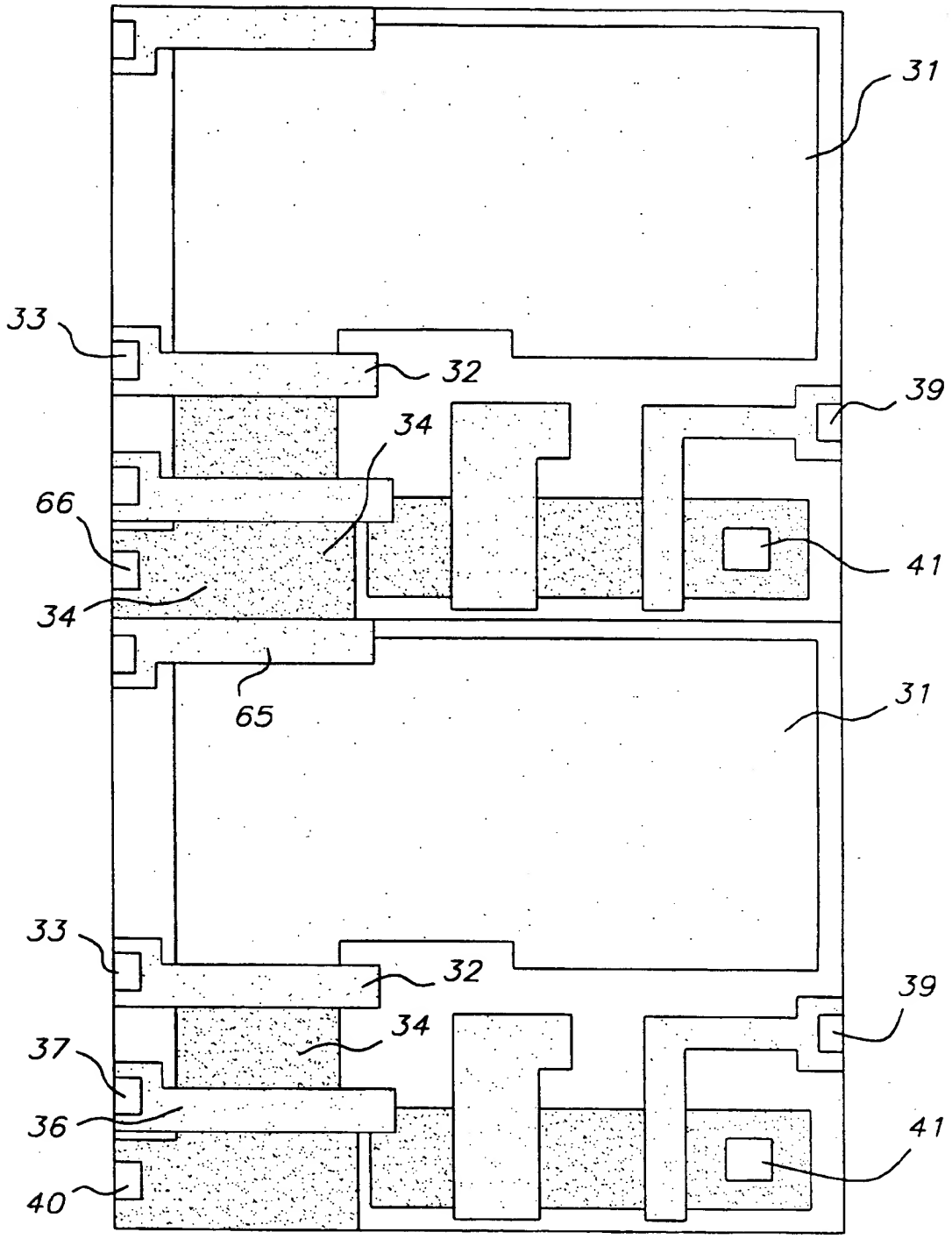

FIG. 7

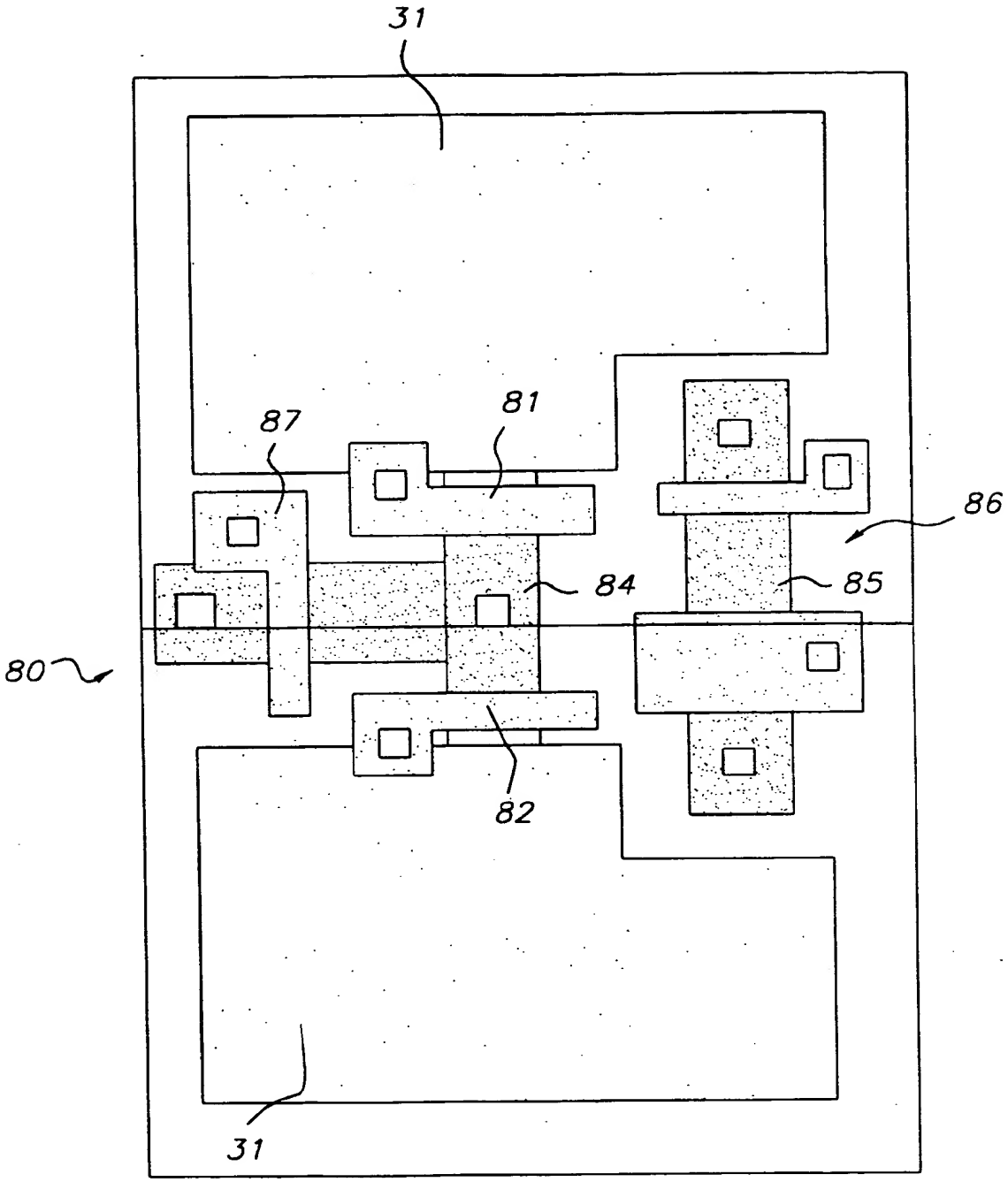

FIG. 8

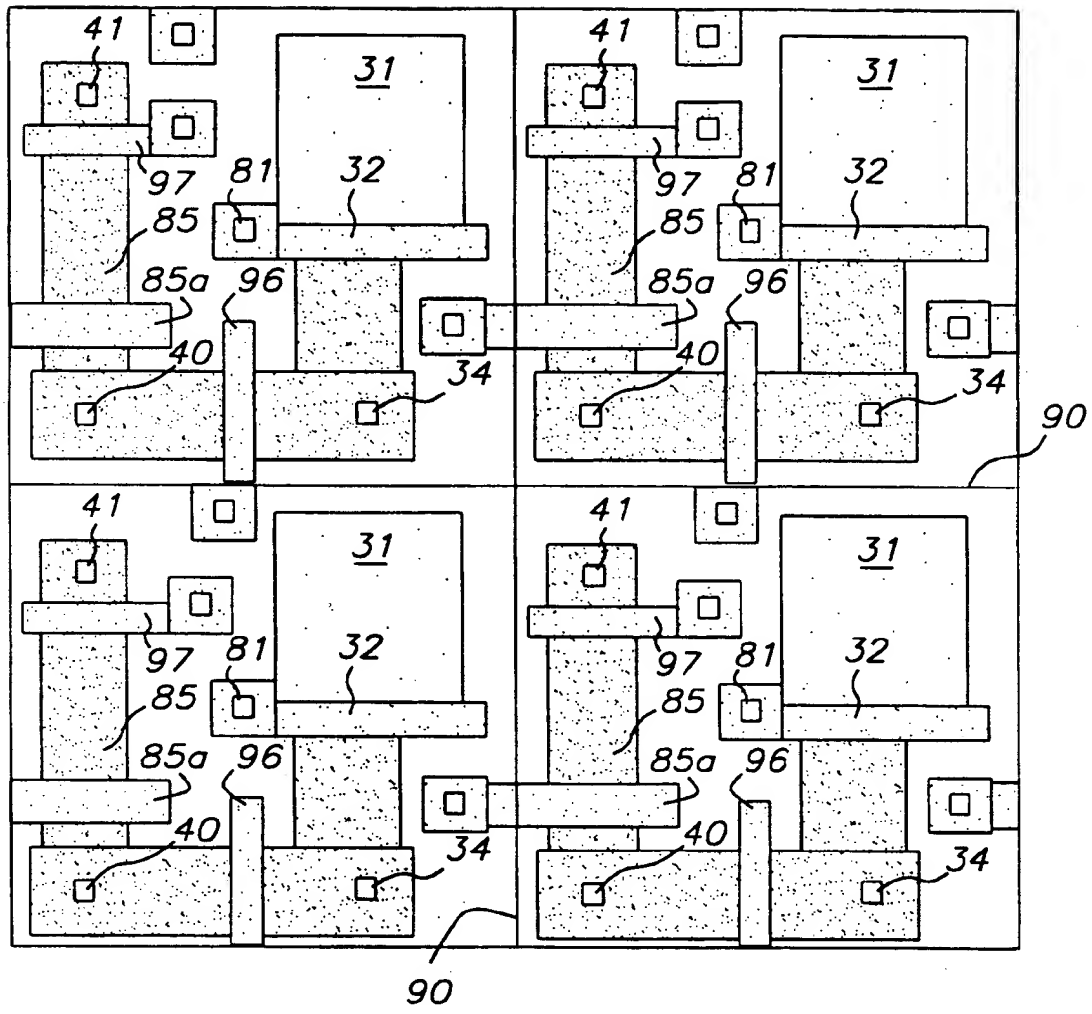

FIG. 9

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 862 219 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
13.01.1999 Bulletin 1999/02

(43) Date of publication A2:
02.09.1998 Bulletin 1998/36

(21) Application number: **98200441.8**

(22) Date of filing: **12.02.1998**

(51) Int. Cl.[6]: **H01L 27/146**, H04N 3/15

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **28.02.1997 US 808444**

(71) Applicant: **EASTMAN KODAK COMPANY**
Rochester, New York 14650 (US)

(72) Inventor:
Guidash, Robert Michael,
c/o Eastman Kodak Company
Rochester, New York 14650-2201 (US)

(74) Representative:
Parent, Yves et al
KODAK INDUSTRIE,
Département Brevets,
CRT - Zone Industrielle
71102 Chalon-sur-Saône Cedex (FR)

(54) Active pixel sensor in which adjacent pixels share an integrated electrical element

(57) An image sensor having a plurality of pixels comprising a semiconductor material of a first conductivity type with at least two adjacent pixels, each of the pixels has a photodetector (31) formed within the substrate and an electrical element that is shared between the adjacent pixels integrated within the adjacent pixels. The electrical element can be: a transfer gate, a reset gate, a row select gate, an amplifier drain, an output node, a floating diffusion, a reset drain, a lateral overflow gate, an overflow drain or an amplifier, that is shared between multiple pixels resulting in a saving of space.

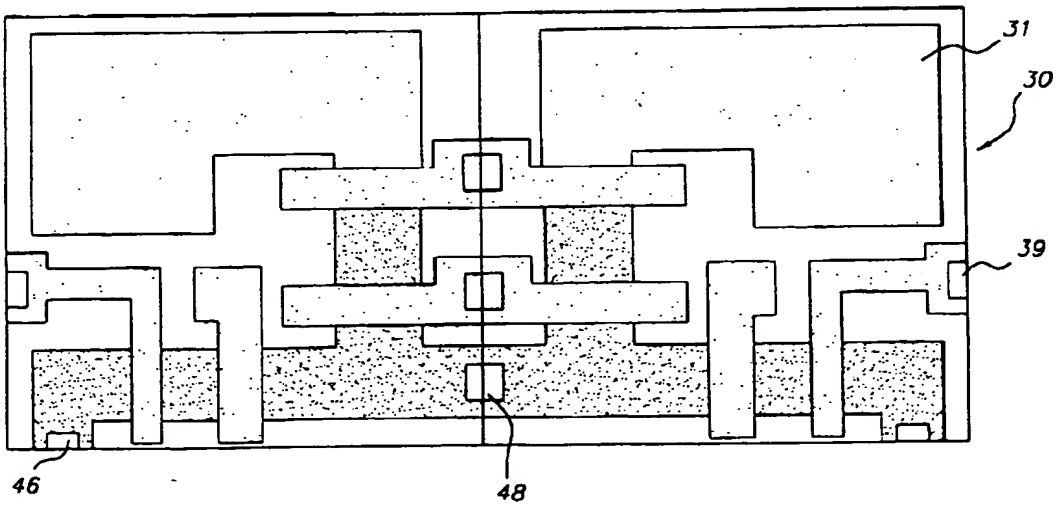

FIG. 4A

EP 0 862 219 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 20 0441

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 4 636 865 A (IMAI MASAHARU) 13 January 1987 * figures 4,5,5,9,12 * * column 4, line 55 - column 5, line 56 *	1-3,5,7, 9,10	H01L27/146 H04N3/15
A	---	6	
X	EP 0 757 476 A (CANON KK) 5 February 1997 * abstract; figure 2 * * column 2, line 49 - column 3, line 36 * * column 4, line 36 - line 48 * * column 6, line 31 - line 43 *	1-3,5,7, 9,10	
X	---		
	PATENT ABSTRACTS OF JAPAN vol. 013, no. 081 (E-719), 23 February 1989 -& JP 63 261744 A (OLYMPUS OPTICAL CO LTD), 28 October 1988 * abstract *	1,2,4	
X,P	---		
	WO 97 42661 A (LITTON SYSTEMS CANADA ;HUANG ZHONG SHOU (CA)) 13 November 1997 * page 4, line 13 - line 20 * * page 5, line 7 - line 13 * * page 6, line 14 - page 7, line 3 * * page 14, line 13 - line 31 * * claims 1,2,4,5 *	1,3,9,10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 November 1998	Visscher, E

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)